

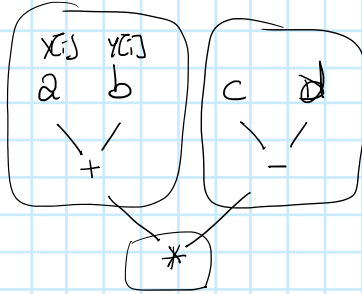
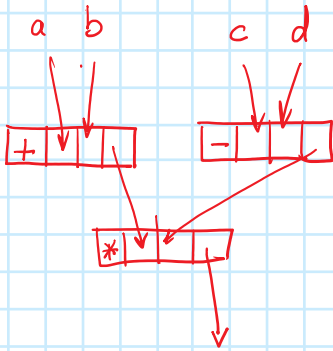
# DATA FLOW

$$x[i] \quad y[i]$$

$$(a+b) * (c-d)$$

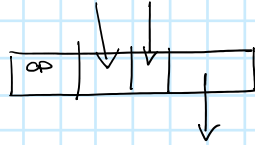
$$\begin{array}{ccc} t_1 & * & t_2 \\ \hline & & \hline & & - \end{array}$$

- ② | LOAD x[i] →
- LOAD y[i] →
- ADD R1
- ① | SUB c-d R2
- ③ | MUL

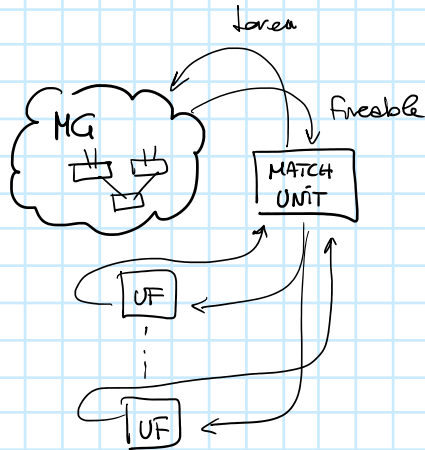
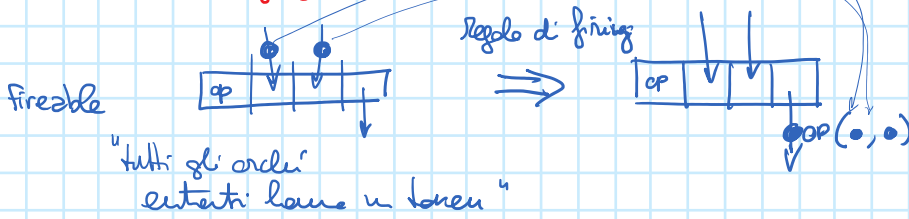


## GRAFO DATA FLOW

Istruzioni DF

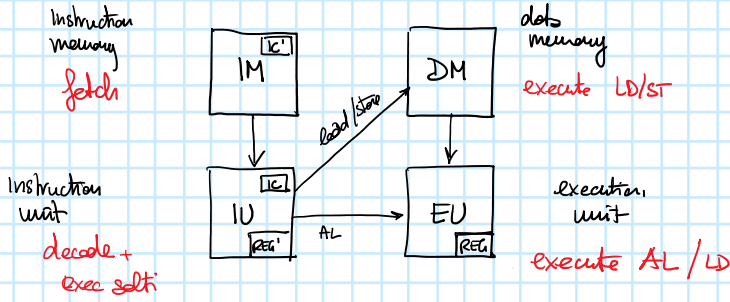


## "Calcolo" di un grafo DF



# PROCESSORE D-RISC "PIPELINE" (HARVARD)

mercoledì 29 novembre 2017 09:35



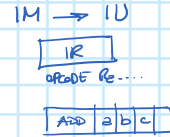
SAZI: IM → IU  

load	a
------	---

IU  
 $R_B \rightarrow IC$   
 made ad IM il nuovo valore di IC



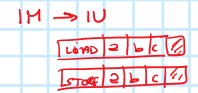
ADD



IU decodifica  
 → EU  
 <+, a, b, c>

EU  
 $R_a + R_b \rightarrow R_c$

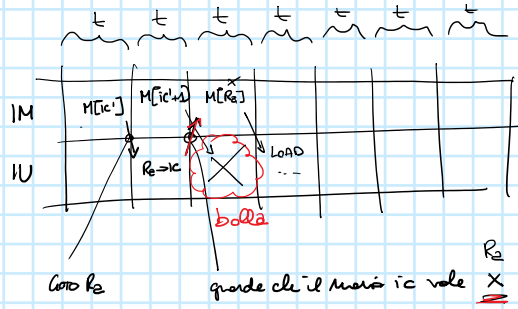
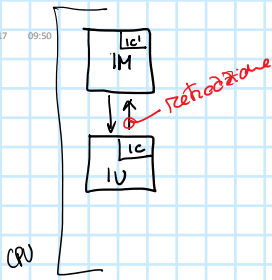
LOAD STORE



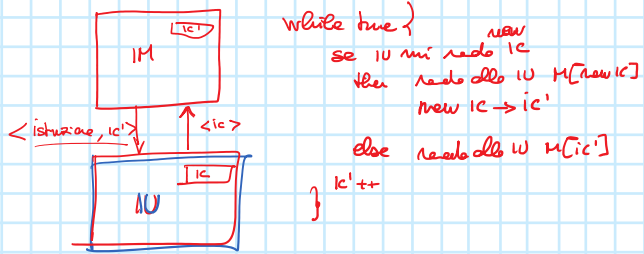
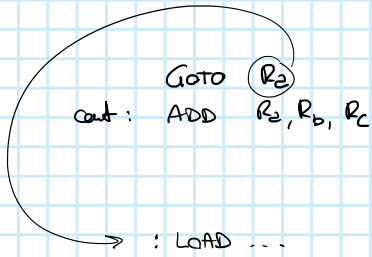
IU decodifica  
 $R_a, R_b$   
 <"LD", ind, R<sub>c</sub>> → DM  
 <"ST", ind, val> → EU  
 <"LD", R<sub>c</sub>>

DM esegue op richieste  
 per LD invia a EU  
 <val>

EU  
 IU → <"ld", c>  
 EU → <val> } val → R<sub>c</sub>

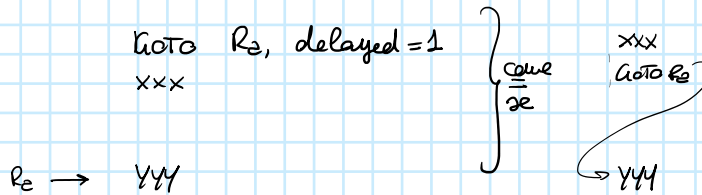


← tempo di servizio (o latenza, tanto IM ed IU sono sequenziali) di IM ed IU

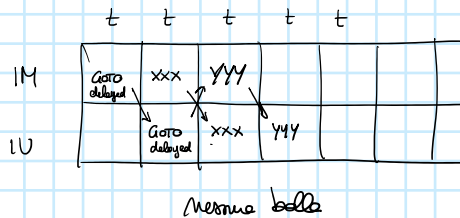


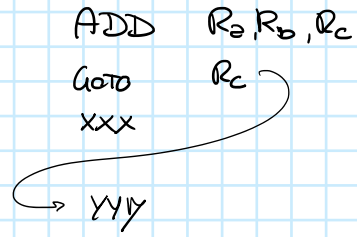
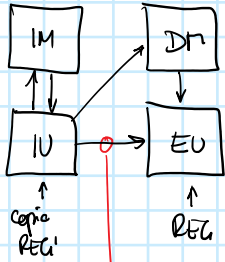
```
while (true) {
    ...
    if (<istruzione, ic'>. ic' == ic)
        then (decalcia <istruzione, ic'>. istruzione)
    else nop
}
```

delayed branch



esse "Bernstein"  
xxx non altera registro perché è la istruzione di salto





$\langle op, a, b, c \rangle \Rightarrow EU: \text{fai } (R_a) \text{ op } (R_b) \rightarrow (R_c)$

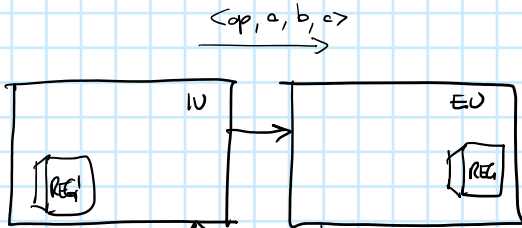
il valore di  $R_c' \neq R_c$  dello EU

	0	1	2	3	4	5	6	7	8	9
IM	A	G								
IU		A	G							
DM										
EU			A							

scelto  $R_c$

$\langle +, d, b, c \rangle$

rendiamo il problema



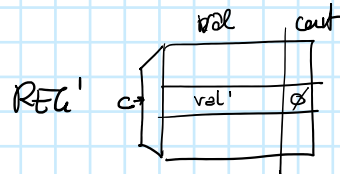
reazione EU-IU

nuovi valori di reg

$\langle c, val \rangle$

	0	1	2	3	4	5
IM	X	G	xxx	xxx	yyy	
IU		A	G	G	xxx	yyy
DM						
EU			A			

$\langle c, val \rangle$



esse IU manda  $\langle op, - - c \rangle$  ad EU

$cont(c)++$

quando IU legge  $R_c$

se  $cont(R_c) \neq 0 \Rightarrow$  <sup>si</sup> blocca

ADD  $R_a, R_b, R_c$   
 GOTO  $R_c$   
 XXX  
 → YYY

*bello davanti a "dipendenza logica" valore di leggere su Unità X quando scritto da Unità Y*

ogni volta che arriva  $\langle val, x \rangle$  dal canale retrocede EU  $\rightarrow$  IU

$val \rightarrow Reg'[x]. \text{valore}$   
 $Reg'[x]. \text{cont} --$

	0	1	2	3	4	5	6	7	8	9
IM	A	G	xxx		yy					
IU		A	G	C	xxx	yy				
DM										
EU			A							

IU 1) Manda a EU  $\langle +, a, b, c \rangle$   
 2)  $cont(R_c)++$

EU  $\rightarrow$  IU  $\langle val, c \rangle$

IU  $val \rightarrow Reg'[c]. \text{valore}$   
 $Reg'[c]. \text{cont} --$

*bello "do salto"*

*esecuzione del programma*

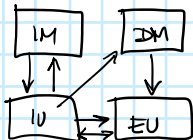
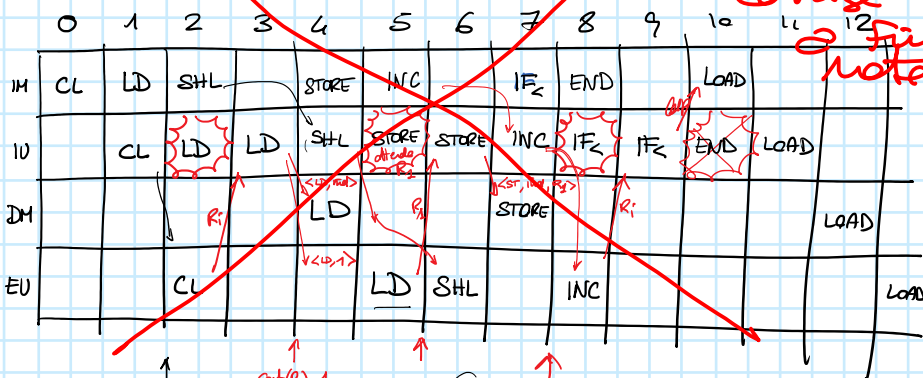
```
for(i=0; i<N; i++) a[i] = b[i] * 2;
```

*vedi anche  
consegne  
fine  
note*

*Tid = 6t*

```

t CLEAR R1
Loop: t LOAD RbaseB, R1, R1
t SHL R1, #1, R1
t STORE RbaseA, R1, R1
t INC R1
t IFZ R1, RN, Loop
END
    
```



$$e = \frac{6t}{10t} = 0.6$$

*Tid*  
*T(n)*

tempo di completamento del codice:  $n$  it + 1<sup>a</sup> iterazione }  $10t$  in questo caso

2 problemi  
 "balle da salto"

"balle da dipendere logico"

SOLUZIONI

```
loop: SUB Ri, #1, Ri
```

```
ADD R0, R0, RC
IFC RC, RN, loop
```

k=1  
loop+1

usare delayed branch



Strutturare codice assembler  
 D-RISC

A	IF <sub>C</sub>		
A	IF <sub>C</sub>	IF <sub>C</sub>	
	A		

A	S	IF <sub>C</sub>	
A	S	IF <sub>C</sub>	
	A	S	

3t x 2ist  
 E = 2/3

3t x 3ist  
 E = 1

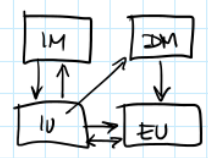
ERRATA CORRIGE (esecuzione programma for(i=0; i<N; i++) a[i] = b[i]\*2;)

Tid = 0t

```

t CLEAR Ri
loop: t LOAD RbaseB, Ri, R1
t SHL R1, #1, R2
t STORE RbaseA, Ri, R2
t INC Ri
t IFZ Ri, RN, loop
END
    
```

	0	1	2	3	4	5	6	7	8	9	10	11	12
M	ADD	LD		SHL	ST			INC	IF <sub>Z</sub>		END	LD	
IU		ADD	LD	LD	SHL	ST	ST	ST	INC	IF <sub>Z</sub>	IF <sub>Z</sub>	END	LD
DM					LD				ST				
EU			ADD			LD	SHL			INC			



↑ out(R<sub>i</sub>)=1    ↑ out(R<sub>i</sub>)=0    ↑ out(R<sub>i</sub>)=1    ↑ out(R<sub>i</sub>)=0    ↑ out(R<sub>i</sub>)=1  
 ↑ out(R<sub>i</sub>)=0    ↑ out(R<sub>i</sub>)=1  
 dip EU-IU (ADD → LD)  
 dip EU-IU (SHL → ST)